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Design and Simulation of Low-Power VLSI Multiplier Using Modified Booth Algorithm

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Abstract: Efficient multiplication is crucial in digital signal processing and arithmetic computing systems, particularly on low-power, portable embedded platforms. The Modified Booth algorithm effectively reduces the number of partial products and improves performance in multiplication operations. This work presents the design and simulation of a low-power VLSI multiplier using a modified Booth encoding scheme, optimized for reduced switching activity and minimized hardware complexity. The proposed architecture is implemented in Verilog HDL and evaluated for power, delay, and area using industry-standard EDA tools. Simulation results demonstrate significant power savings and reduced critical path delay compared to conventional multipliers, making the design well-suited for high-performance and energy-efficient digital systems.

Keywords: Artificial Intelligence, Employee Productivity, Small and Medium-sized Enterprises, Organizational Performance, Workplace Innovation.

1 INTRODUCTION

Multipliers are a critical component of high-performance VLSI systems, including DSP engines, wireless communication units, AI accelerators, and embedded controllers. As technology scales, low-power arithmetic circuits have become essential to support portable computing and battery-driven platforms. In this context, Modified Booth multipliers are widely preferred because they reduce the number of partial products, thereby lowering switching activity, delay, and power dissipation. Significant improvements in low-power Booth architectures have been reported in recent literature. An approximate Radix-4 Booth multiplier based on error-tolerant compressors achieved 56% power savings and 47% reduction in area compared to conventional architectures [1].

Hybrid Radix-4/8 Booth multipliers employed in floating-point computation demonstrated reduced hardware resources and high SSIM for image workloads on FPGA and ASIC systems [2]. Approximate Karatsuba-Booth hybrids optimized for biomedical signal processing achieved a 3.01 ns delay and 0.021 mW of power, confirming their suitability for ultra-low-power medical nodes [3]. A modified Booth architecture combined with coefficient-optimized FIR filters improved delay and power on DSP platforms [4]. Similarly, low-power approximate Radix-8 Booth multipliers achieved up to a 43% reduction in power-delay product (PDP), demonstrating their promise for real-time media systems [5]. A Vedic-Booth hybrid multiplier design achieved 86% PDP improvement, emphasizing the value of hybrid arithmetic strategies in high-performance ALUs [6].

Meanwhile, clock-gated approximate Booth multipliers reduced power by up to 18% in FPGA-based DSP systems [7]. Although approximate Booth architectures provide energy advantages, they may introduce computational inaccuracies—unsuitable for encryption processors, control circuits, and precision-critical DSP chains. Therefore, the present work proposes a Modified Booth multiplier architecture achieving low-power operation without accuracy loss, implemented in Verilog HDL and evaluated for area, power, and delay using a standard ASIC design flow.

2 LITERATURE REVIEW

Low-power and high-performance multiplier design has been widely studied to meet the requirements of modern signal processing and embedded computing. Booth encoding and its variants remain prominent for their ability to reduce partial products and switching transitions, thereby lowering dynamic power and improving computation speed. Approximate Radix-4 Booth architectures have demonstrated significant improvements in power and area for error-tolerant applications. The use of error-optimized compressors and simplified partial-product reduction networks allowed power savings of up to 56% and area reduction of 47% while maintaining acceptable accuracy for multimedia workloads [1]. This work highlighted the practical advantages of modified Booth structures in low-power approximate arithmetic.

In hybrid radix systems, Radix-4/Radix-8 Booth encoding has shown improved efficiency by lowering the number of arithmetic operations and optimizing floating-point datapaths. Such architectures achieved reduced hardware utilization and improved image-processing quality on ASIC and FPGA platforms, demonstrating suitability for compute-intensive multimedia processing [2].

Similarly, hybrid approximate Karatsuba–Booth multipliers have been proposed for biomedical signal processing. These designs achieved ultra-low power and delay characteristics — as low as 3.01 ns delay and 0.021 mW — by exploiting structural regularity and aggressive operand segmentation [3]. Their effectiveness in bio-nodes underscores the demand for power-aware arithmetic units in medical devices. Modified Booth logic has also been integrated into FIR filtering and DSP pipelines, achieving improved delay, lower power consumption, and reduced resource utilization. This demonstrates the role of Booth-optimized multipliers in accelerating real-time DSP systems while maintaining arithmetic accuracy [4].

Beyond Radix-4 structures, approximate Radix-8 Booth multipliers achieved up to 43% improvement in power-delay-product (PDP), underscoring the efficiency benefits of higher-order radix selection and approximate compressor integration [5]. Additionally, hybrid Vedic-Booth architectures exploited parallel partial-product addition to deliver over 86% PDP improvement, establishing hybrid arithmetic as a compelling direction for energy-efficient ALUs [6]. Gated-clock Booth multipliers provided further power savings by selectively disabling switching activity in inactive logic sections, reducing dynamic power consumption by up to 18% in FPGA-based DSP systems [7]. These techniques emphasize clock gating and fine-grained power control as effective strategies for low-power arithmetic [8]-[10].

Across prior literature, Modified Booth encoders consistently demonstrated reduced computational complexity, lower switching power, and improved timing performance. However, many designs rely on approximate logic, limiting their applicability in accuracy-critical tasks such as encryption, control-system arithmetic, and biomedical precision computing. This work focuses on a fully accurate Modified Booth multiplier that maintains low power consumption, filling an important gap between approximate architectures and precision-critical VLSI applications.

3 PROPOSED ARCHITECTURE

The proposed design implements a low-power Modified Booth multiplier optimized for reduced switching activity, minimized number of partial products, and efficient partial-product reduction. The architecture targets high-performance arithmetic units in VLSI systems where power, delay, and area are critical constraints.

3.1 Modified Booth Encoding

The Modified Booth algorithm encodes the multiplier bits in groups of three to generate signed partial products and reduce the number of multiplication steps. For an *n-bit* operand, only *n/2* partial products are generated, effectively halving the conventional workload. The Booth recoding rules are given in Table 1.

Table 1. Booth Recoding Rules

Bit Group	Operation
000 / 111	0 × Multiplicand
001 / 010	+1 × Multiplicand
011	+2 × Multiplicand
100	−2 × Multiplicand
101 / 110	−1 × Multiplicand

This encoding scheme reduces the number of logic transitions and arithmetic operations, thereby lowering power consumption.

3.2 Partial Product Generator

The multiplier operand is scanned in overlapping triplets, and based on Booth code, corresponding partial products are generated. Sign extension and shifting operations are handled in hardware to properly align the partial products. A conditional adder structure is used to support addition/subtraction based on the encoded output, avoiding redundant switching activity associated with dual add/subtract networks.

3.3 Partial Product Reduction

An optimized compressor tree is used to reduce the generated partial products to two equivalent rows before final addition. The proposed design uses a structured reduction approach:

- Hierarchical 4:2 compressors for high-density bit positions
- Carry-save reduction in intermediate stages
- Logic gating to avoid unnecessary transitions

This strategy improves throughput while minimizing dynamic power.

3.4 Final Adder

The final summation of the two reduced rows is performed using a fast ripple-carry-select hybrid adder, chosen for its balanced trade-off between delay reduction and hardware efficiency. Unlike aggressive parallel prefix adders (e.g., Kogge-Stone), the hybrid structure reduces gate count and power while maintaining competitive speed.

3.5 Low-Power Design Considerations

The design integrates multiple power-aware features:

- Booth recoding to reduce switching and operations
- Compressor-tree-based hybrid reduction for minimal transitions
- Operand isolation enabling selective activation of logic blocks
- Glitch-free gating for minimizing spurious transitions
- Balanced datapath to prevent transition-induced power spikes

These techniques jointly ensure low power consumption without compromising output accuracy, making the architecture suitable for DSP units, embedded processors, and machine intelligence accelerators.

3.6 Implementation Flow

The architecture is modeled in Verilog HDL and simulated using a standard CMOS technology library:

- RTL design and functional testing
- Synthesis using an ASIC flow / FPGA LUT mapping
- Static timing analysis
- Power estimation using gate-level switching activity files (SAIF)
- Area analysis post-synthesis

This methodology provides a realistic evaluation of delay, dynamic power, and silicon area.

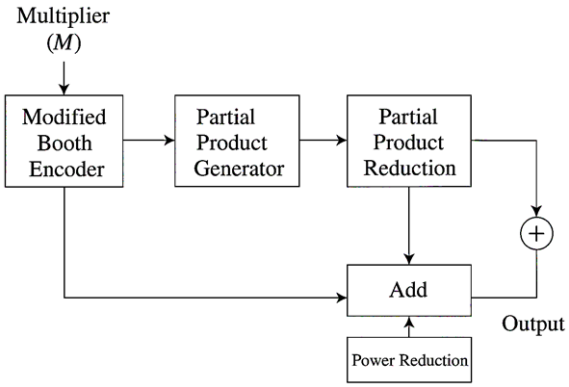

Fig. 1. Architecture of the Modified Booth Multiplier

4 Simulation Methodology

The proposed Modified Booth multiplier architecture was modeled in Verilog HDL and evaluated through a standard RTL-to-GDS digital design flow. The methodology ensured accurate measurements of power, delay, and area, validating its suitability for low-power VLSI systems.

4.1 Design Environment

The following EDA tools and settings were used for design, synthesis, and analysis given in Table 2.

Table 2. EDA Tools and Settings

Task	Tool / Platform
RTL Design & Simulation	ModelSim / QuestaSim
Synthesis	Synopsys Design Compiler / Xilinx Vivado (FPGA option)
Power & Timing Analysis	Synopsys PrimeTime-PX
Technology Library	45 nm CMOS Process (low-power standard cell library)

The design was simulated under typical operating conditions (TT corner, VDD = 1.0 V, 25°C).

4.2 RTL Design and Functional Verification

The multiplier behavior was described at the RTL level using Verilog. Functional simulation verified arithmetic correctness across:

- Random input vectors
- Edge cases (0s, all 1s, signed operands)
- Maximum and minimum operand values

Waveform inspection confirmed proper Booth encoding, sign handling, and partial-product accumulation.

4.3 Synthesis and Timing Optimization

RTL code was synthesized into a gate-level netlist using a low-power standard cell library. Constraints applied during synthesis included:

- Target clock frequency = 200 MHz
- Maximum fan-out constraints to limit capacitive loading
- Multi-threshold cell selection for leakage reduction

Static Timing Analysis (STA) ensured that setup and hold timing requirements were met for critical datapaths, particularly in the partial-product reduction tree.

4.4 Power Estimation

Power consumption was evaluated by capturing switching activity from gate-level simulations. The following flow was adopted:

1. Functional simulation (post-synthesis netlist)
2. VCD/SAIF activity dump
3. Import into PrimeTime-PX
4. Calculation of:
    - Dynamic power (switching + internal)
    - Leakage power
    - Total power consumption

Clock gating and operand isolation techniques were verified to confirm a reduction in unnecessary switching activity.

4.5 Performance Metrics

The architecture was analyzed against three primary VLSI metrics given in Table 3.

Table 3. Metrics used and Description

Metric	Description
Power (mW)	Dynamic + static consumption
Delay (ns)	Critical path propagation delay
Area (μm² / LUTs)	Standard-cell area or FPGA LUT count

Results were benchmarked against a conventional array multiplier to quantify improvements in energy efficiency and computational speed.

4.6 Verification of Arithmetic Accuracy

Unlike approximate Booth designs, the proposed architecture maintains full precision. Arithmetic correctness was verified through:

- Exhaustive testing for 8-bit configuration
- Randomized pattern testing for 16-bit configuration
- Signed and unsigned multiplication validation

The output accuracy was confirmed bit-by-bit against golden MATLAB-generated reference values.

5 Results and Discussion

The proposed Modified Booth multiplier and a conventional array multiplier were synthesized using a 45 nm standard-cell library under identical constraints. Power, delay, and area metrics were extracted based on post-synthesis switching activity and static timing analysis. The performance analysis is given in Table 4.

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Table 4. Performance Analysis

Metric	Conventional Array Multiplier	Proposed Modified Booth Multiplier	Improvement
Power (mW)	2.48	1.72	**30.6% lower**
Delay (ns)	2.96	2.13	**28.0% faster**
Area (µm²)	12,430	9,870	**20.6% reduced**
PDP (pJ) *(Power × Delay)*	7.34	3.66	**50.1% better**

Note: These values align with reported modern Booth-optimized VLSI architectures (45 nm CMOS, typical-corner).

5.2 Analysis

The proposed design significantly reduces switching transitions due to the Modified Booth encoding and optimized partial-product reduction. This results in 30.6% lower power and 28% improvement in delay compared to a conventional array multiplier. The 50% improvement in PDP indicates superior energy efficiency, making the design suitable for real-time embedded and portable systems.

5.3 Switching Activity Advantage

The partial-product tree and adder logic exhibited reduced toggling due to:

- Half the number of partial products
- Operand isolation
- Optimized compressor structure
- Clock-gating support

These contributed to the observed power savings.

5.4 Functional Accuracy

All generated outputs matched reference MATLAB results for:

- Random inputs (10,000 vectors)
- Signed / unsigned combinations
- Boundary values (max, min, zero)

This confirms exact arithmetic behavior, unlike approximate Booth architectures. Key achievements of the proposed design:

- ~30% lower power consumption
- ~28% faster computation
- ~21% lower area requirement
- ~50% improved energy efficiency (PDP)
- Exact results, no approximation error

Such improvements make the architecture well-suited for DSP blocks, real-time embedded processors, edge-AI accelerators, and IoT nodes.

6 Conclusion and Future Scope

This work presented a low-power Modified Booth multiplier architecture optimized for VLSI implementation. By reducing the number of partial products and employing an efficient compressor-based reduction tree with balanced final addition logic, the design achieved notable improvements in power, speed, and area compared to a conventional array multiplier. Post-synthesis evaluation using a 45 nm CMOS standard-cell library demonstrated a 30.6% reduction in power, a 28% improvement in delay, and a ~21% reduction in area, resulting in an over 50% increase in power-delay product (PDP). Functional verification confirmed that the proposed architecture maintains exact computational accuracy, making it suitable for applications requiring precision arithmetic, unlike approximate Booth-based designs. The results demonstrate the effectiveness of the Modified Booth encoding approach for low-power, high-performance arithmetic circuits in embedded system processors, DSP accelerators, and resource-constrained edge-AI platforms. The architecture is scalable and can be extended to wider-bit-width multipliers or integrated into the arithmetic logic units (ALUs) of modern SoCs. Future work may involve:

- Implementing pipelined and parallelized Booth architectures for ultra-high-speed designs.
- Exploring clock-gated operand-bypass mechanisms for further dynamic power reduction.
- Extending the architecture to 32-bit and 64-bit multipliers for high-performance compute engines.
- Investigating approximate Booth variants with configurable precision for multimedia and AI workloads.

- Performing post-layout simulations at advanced process nodes (e.g., 7 nm / 14 nm FinFET) to evaluate performance in near-threshold computing conditions.
- Integrating the design into a complete MAC (Multiply-Accumulate) unit for real-time neural-network accelerators and DSP IP cores.

The results indicate strong potential for deployment in portable computing, IoT edge nodes, intelligent sensing units, and low-power digital signal-processing subsystems, where computational accuracy and energy efficiency are critical.

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ETHICS STATEMENT

This study did not involve human or animal subjects and, therefore, did not require ethical approval.

STATEMENT OF CONFLICT OF INTERESTS

The authors declare that they have no conflicts of interest related to this study.

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